OptiMOS®2 Power-Transistor

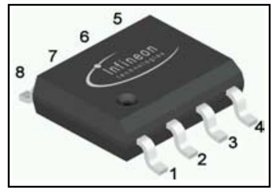
Features

- Fast switching MOSFET for SMPS
- Optimized technology for notebook DC/DC
- Qualified according to JEDEC[1] for target applications
- Dual n-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Avalanche rated
- dv/dt rated
- Pb-free lead plating; RoHS compliant

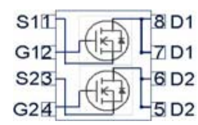
Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	35	mΩ
I_D	6	A

PG-DSO-8



Type	Package	Marking
BSO350N03	PG-DSO-8	350N3



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			10 secs	steady state	
Continuous drain current	I_D	T_A=25 °C[2)]	6	5	A
		T_A=70 °C[2)]	4.8	4	
Pulsed drain current	$I_{D,pulse}$	T_A=25 °C[3)]	24		
Avalanche energy, single pulse	E_{AS}	I_D=6 A, R_{GS}=25 Ω	8		mJ
Reverse diode dv/dt	dv/dt	I_D=6 A, V_{DS}=20 V, di/dt=200 A/µs, $T_{j,max}$=150 °C	6		kV/µs
Gate source voltage	V_{GS}		±20		V
Power dissipation	P_{tot}	T_A=25 °C[2)]	2.0	1.4	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - soldering point	R_{thJS}		-	-	50	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, t_p≤10 s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm^2 cooling area[2)], t_p≤10 s	-	-	63	
		6 cm^2 cooling area[2)], steady state	-	-	90	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=6 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=5 A	-	42	52	mΩ
		V_{GS}=10 V, I_D=6 A	-	29	35	
Gate resistance	R_G		-	0.8	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=6 A	6	12	-	S

[1)] J-STD20 and JESD22

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

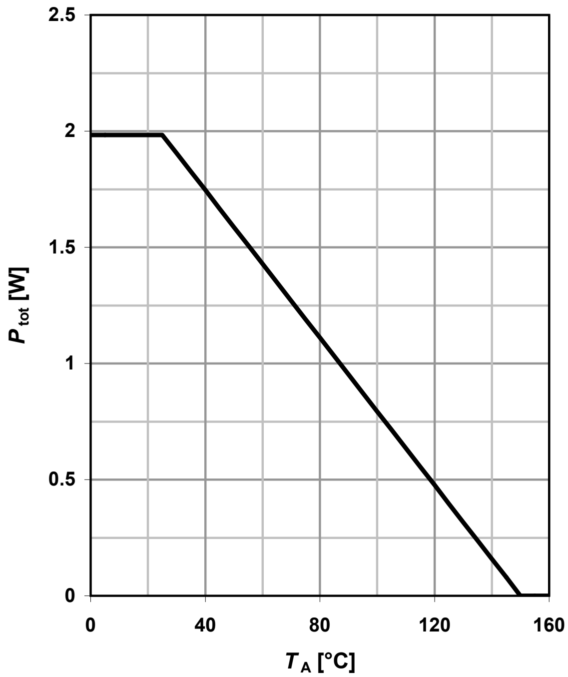
[3)] See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	360	480	pF
Output capacitance	C_{oss}		-	130	170	
Reverse transfer capacitance	C_{rss}		-	19	28	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=3 A, R_G=2.7 Ω	-	2.2	3.3	ns
Rise time	t_r		-	2.2	3.3	
Turn-off delay time	$t_{d(off)}$		-	8.7	13	
Fall time	t_f		-	1.4	2.1	
Gate Charge Characteristics[4]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=3 A, V_{GS}=0 to 5 V	-	1.1	1.4	nC
Gate charge at threshold	$Q_{g(th)}$		-	0.57	0.76	
Gate to drain charge	Q_{gd}		-	0.73	1.1	
Switching charge	Q_{sw}		-	1.2	1.8	
Gate charge total	Q_g		-	2.8	3.7	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	2.4	3.2	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	3.1	4.1	
Reverse Diode						
Diode continous forward current	I_S	T_A=25 °C	-	-	2	A
Diode pulse current	$I_{S,pulse}$		-	-	24	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=2 A, T_j=25 °C	-	0.79	1	V
Reverse recovery charge	Q_{rr}	V_R=12 V, I_F=I_S, di_F/dt=400 A/µs	-	-	3	nC

[4] See figure 16 for gate charge parameter definition

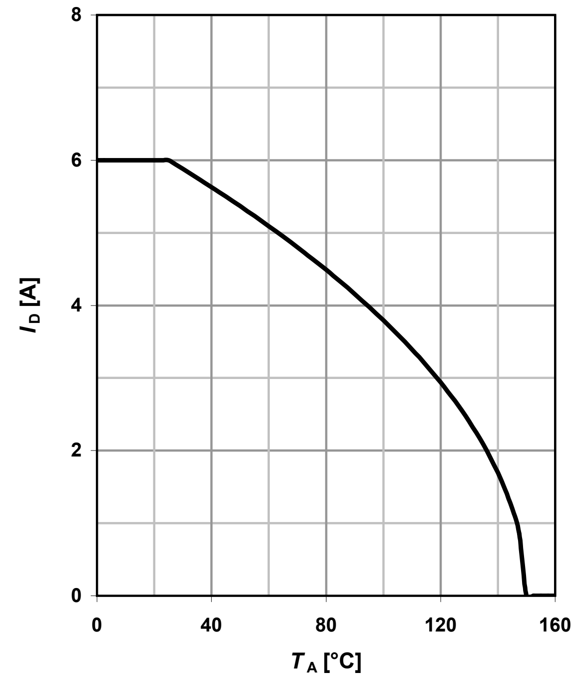
1 Power dissipation

P_{tot}=f(T_A); t_p≤10 s



2 Drain current

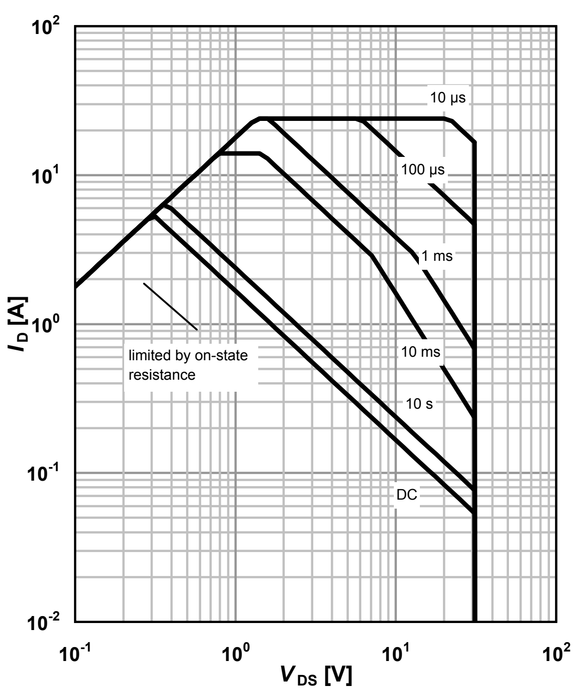
I_D=f(T_A); V_{GS}≥10 V; t_p≤10 s



3 Safe operating area

I_D=f(V_{DS}); T_A=25 °C[1]; D=0

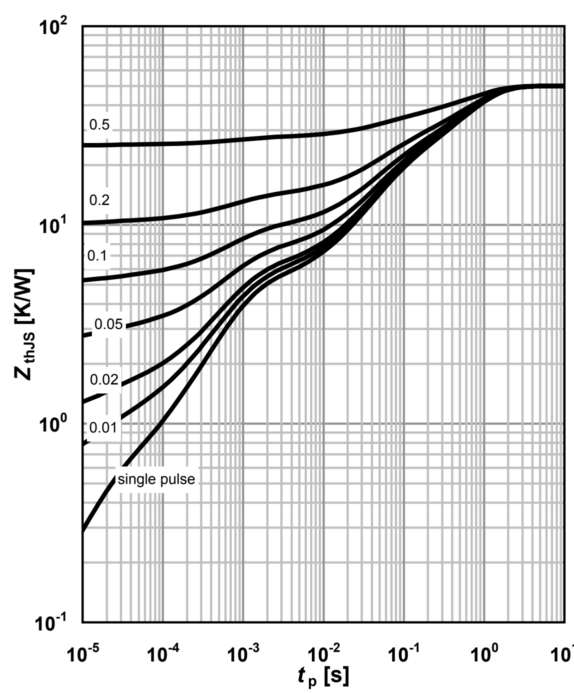
parameter: t_p



4 Max. transient thermal impedance

Z_{thJS}=f(t_p)

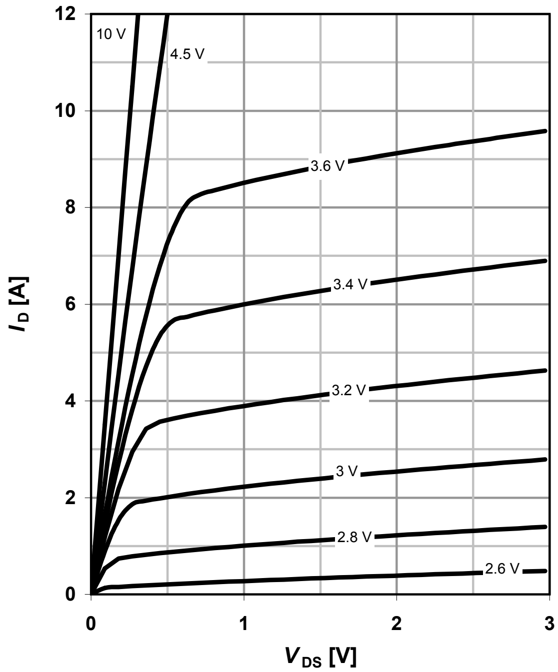
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

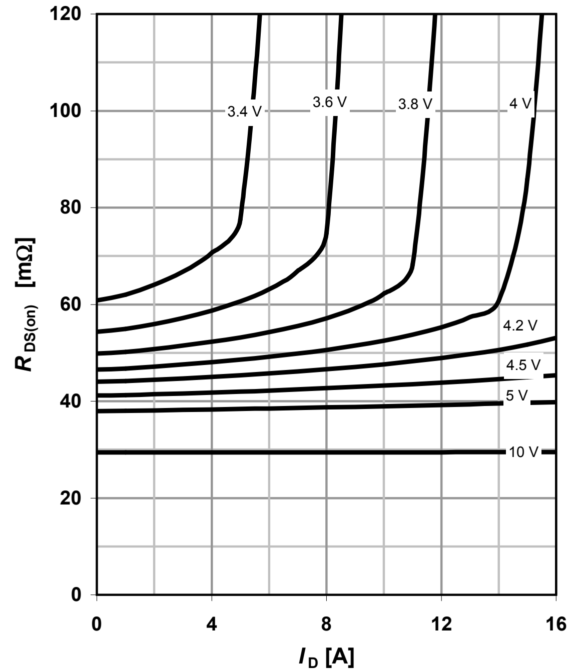
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

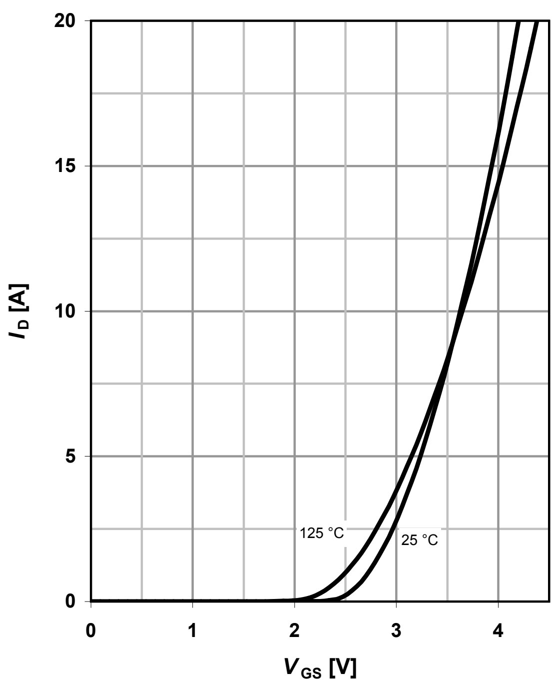
parameter: V_{GS}



7 Typ. transfer characteristics

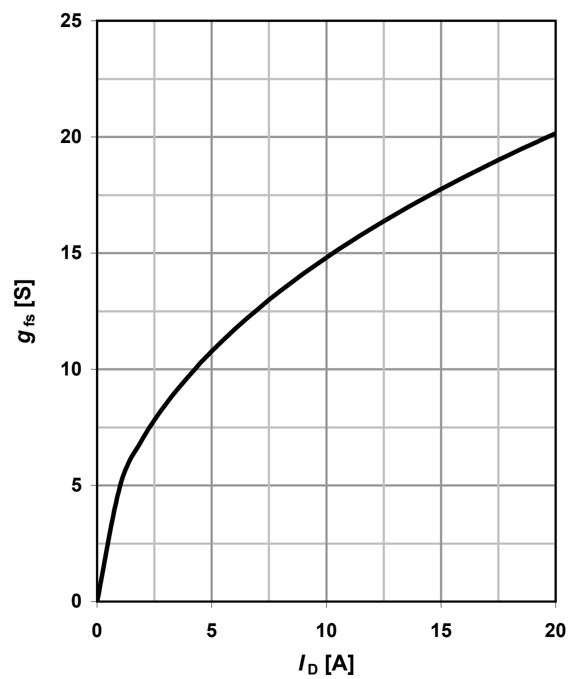
I_D=f(V_{GS}); $|V_{DS}|$>2$|I_D|R_{DS(on)max}$

parameter: T_j



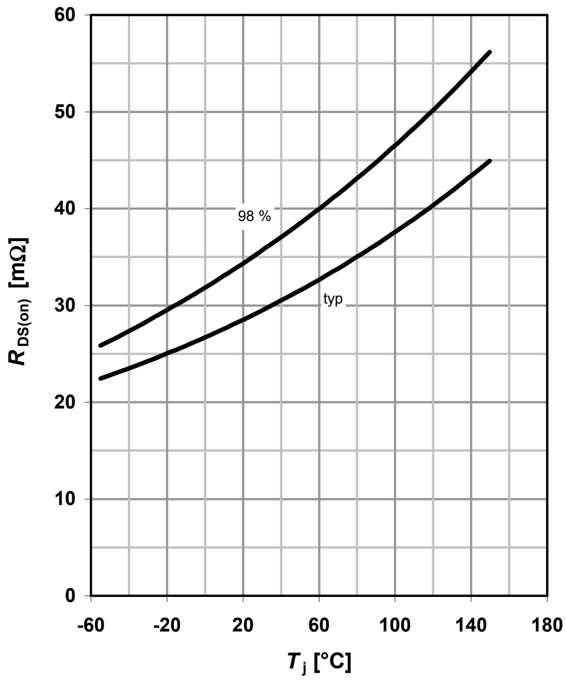
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

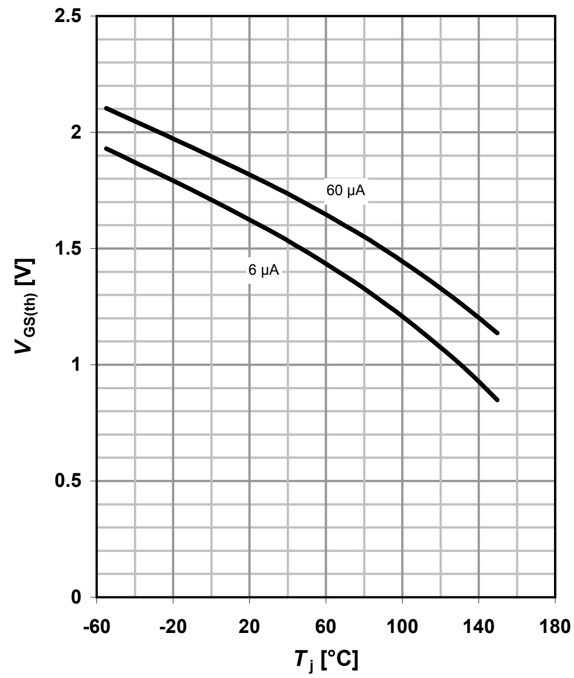
$R_{DS(on)}$=f(T_j); I_D=6 A; V_{GS}=10 V



10 Typ. gate threshold voltage

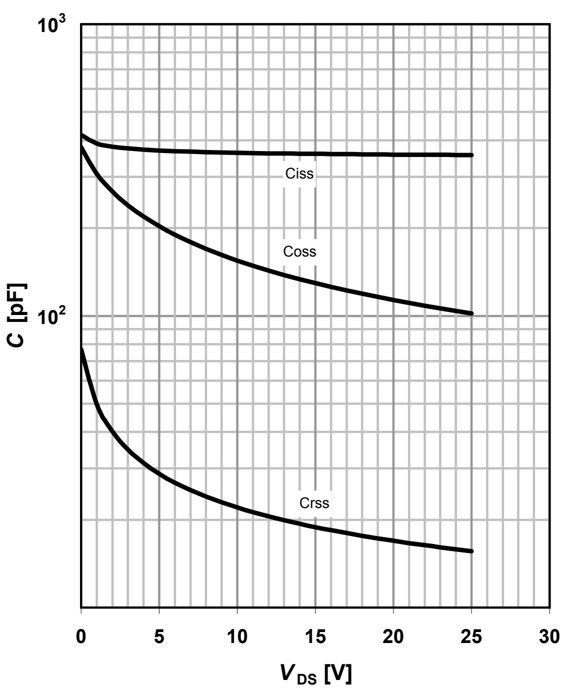
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

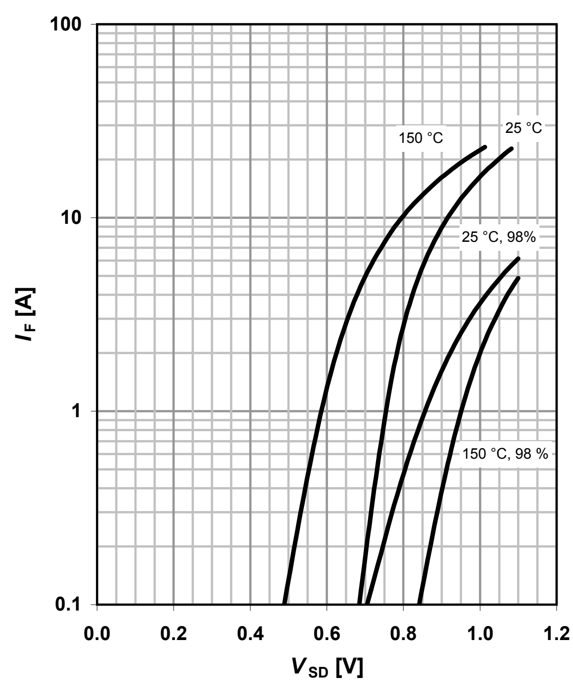
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

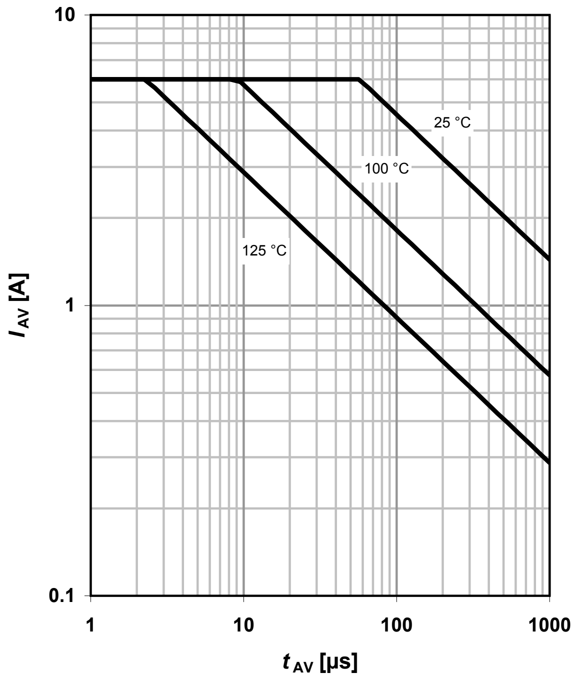
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

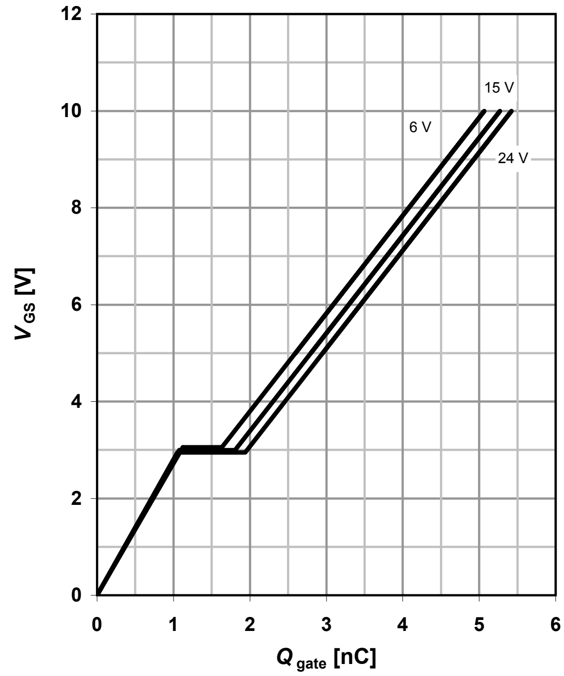
parameter: $T_{j(start)}$



14 Typ. gate charge

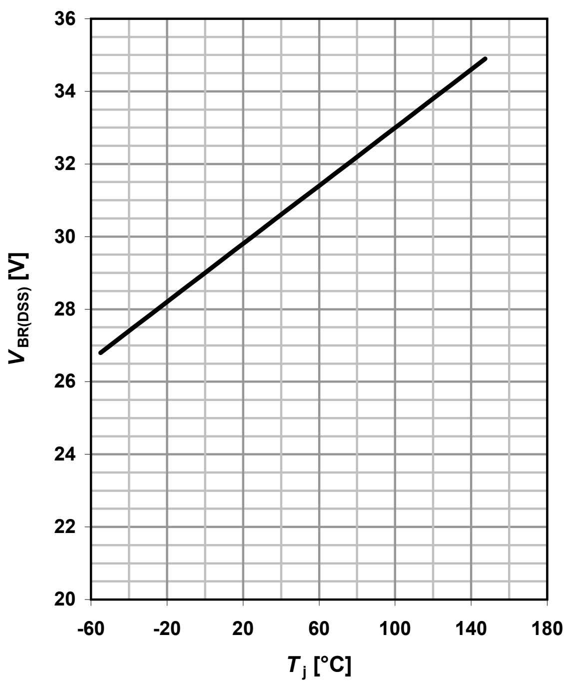
V_{GS}=f(Q_{gate}); I_D=3 A pulsed

parameter: V_{DD}

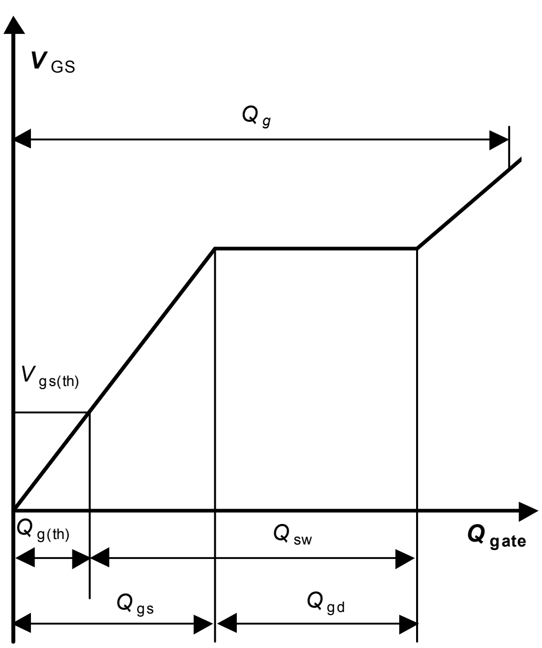


15 Drain-source breakdown voltage

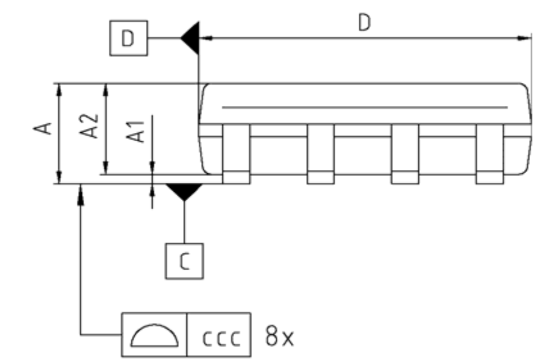
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

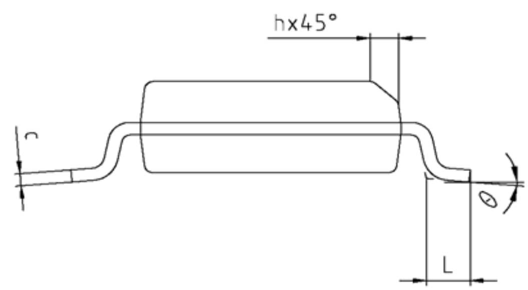


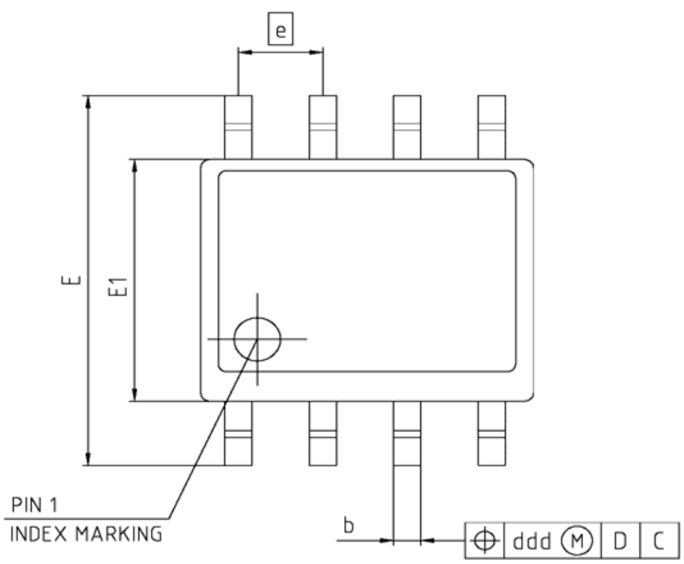
16 Gate charge waveforms



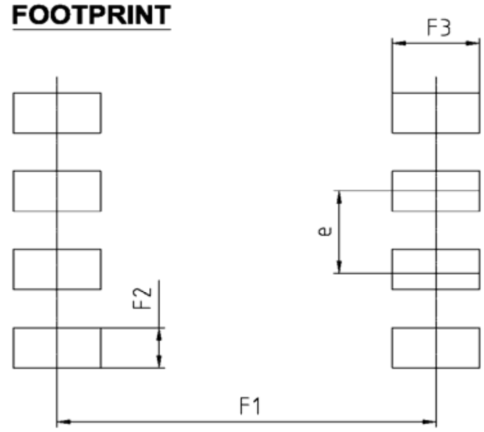
Package Outline **PG-DSO-8**







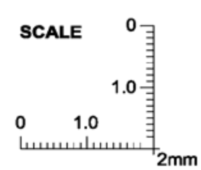
FOOTPRINT



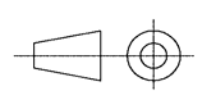
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.750	-	0.069
A1	0.100	-	0.004	-
A2	1.250	1.650	0.049	0.065
b	0.360	0.510	0.014	0.020
c	0.190	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270		0.050	
N	8		8	
L	0.390	0.890	0.015	0.035
h	0.250	0.410	0.010	0.016
Θ	0°	8°	0°	8°
ccc	0.100		0.004	
ddd	0.200		0.008	
F1	5.590	5.790	0.220	0.228
F2	0.550	0.750	0.022	0.030
F3	1.210	1.410	0.048	0.056

REFERENCE
JEDEC / MS-012

SCALE



EUROPEAN PROJECTION



ISSUE DATE
19-09-2005

FILE
DSO-8_1

Published by
Infineon Technologies AG
81726 München, Germany

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